Six-port Direct Digital Receiver (SPDR) and Standard Direct Receiver (SDR) Results for QPSK Modulation at High Speeds

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Abstract — **Comparative measurements on two direct down-conversion receivers are presented to investigate the performance of a six-port digital receiver (SPDR) with a standard direct receiver (SDR) using quadrature zero-IF mixers. The six-port prototype is fabricated in MHMIC format for a carrier frequency of 2.45GHz with QPSK digital modulation suitable for wireless local loop such as WLAN or MMDS systems. BER measurements on both receivers are presented in the presence of noise, adjacent channel and co-channel interference, local oscillator phase shift and sensitivity for 40 Mb/s data rate. MMIC design scheme of the six-port digital receiver can provide a robust, simple, low-cost design platform for use in mass-market communication systems for present and future multimedia broadband applications.**

I. Introduction

The direct down-conversion architecture is very promising in today's wireless world. It offers numerous advantages over standard heterodyne receivers: SAW filters and the second down-conversion stage are replaced with a rather simple high-order low-pass filter without an image problem. Direct conversion receivers reduce dramatically the circuit complexity and facilitate a monolithic implementation [1]. Numerous six-port direct down-conversion receivers have been experimented for different modulation schemes [2]-[6]. The six-port used in this paper is based on a uni-mode distributed parameter design for the ISM microwave frequency band of 2.45 GHz with QPSK digital modulation scheme [7].

Contrary to other six-port software digital receivers [8] using DSPs, this hardware-based architecture ("hardware radio") is less costly and its data rate is limited by the base-band amplifier bandwidth.

This paper presents a direct comparison between a SPDR and a standard direct conversion receiver for multi-purpose applications such as wideband wireless local loop (WLL), wideband direct-sequence-spread-spectrum (DSSS), two-way MMDS or wideband 2.45 GHz ISM digital radios. In these tests the SPDR uses the same components as the SDR except for the six-port circuit.

II. Results on the Direct Down-Conversion Demodulators

A. Standard Zero-IF QPSK Demodulator

Fig. 1 shows a block diagram of the receiver architecture using a "standard" zero-IF demodulator.

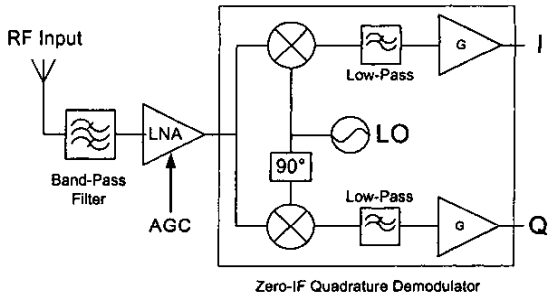

Fig. 1. Direct conversion digital receiver's standard architecture.

Such a typical implementation uses RF filters, a variable gain LNA and a demodulator chip that to provide the I and Q signals for an input RF QPSK signal at 2.45GHz. The chosen demodulator chip is designed for WLLs containing a LNA, and high-speed and high-gain (+80dB) base-band amplifiers. The demodulation is done internally using a standard zero-IF scheme, which consists of two active mixers driven by the RF input signal and a local oscillator signal in phase for "I" signal and in quadrature for the "Q" signal. These two signals are amplified by two stages of wideband high-gain and variable gain integrated amplifiers.

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B. Six-port Digital Receiver (SPDR)

Only the demodulator chip is changed in the chosen architecture as shown in Fig.2. For all tests, the remaining components are the same as for a standard receiver. The demodulator of SPDR has two circuit types: a RF circuit with the six-port and baseband circuits for video amplifier and decoder.

Fig. 2 depicts such a receiver architecture: the six-port has RF and reference signal (LO) inputs and three RF output ports feeding Schottky diode matching circuits to provide baseband signals P_1 P_2 and P_3. In addition, a baseband ancillary module consists of wideband video amplifiers (30MHz) and high-speed comparators with TTL I and Q compatible outputs.

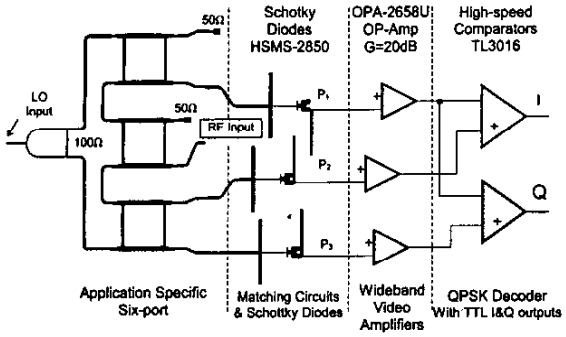

Fig. 2. Prototype of six-port direct digital receiver for QPSK input signals.

C. Test Bench

Today's high performance transceivers must pass more than 100 tests, each representing extreme conditions that may occur in a realistic environment. In these measurements, we do not include the RF filters and the variable gain low-noise amplifier as to restrict all tests to the two different demodulators itself as shown in Fig. 3. It is noted that all tests are done with a synchronized local oscillator in order to obtain the true absolute performance of both receivers. A standard QPSK modulation format is created using a HP vector modulator with the pseudo-random bit sequences (PSBR) given by the bit error rate (BER) transmitter. The local oscillator is derived from the same source as the carrier signal. A QPSK signal feeds the receiver under test and the BER with I & Q outputs are measured.

As the I and Q outputs are analogue in the standard demodulator chip (output of a mixer) and the BER measurement instrument requires TTL or ECL inputs: a simple circuit with high speed comparators (50MHz) was added at the outputs of the standard demodulator chip.

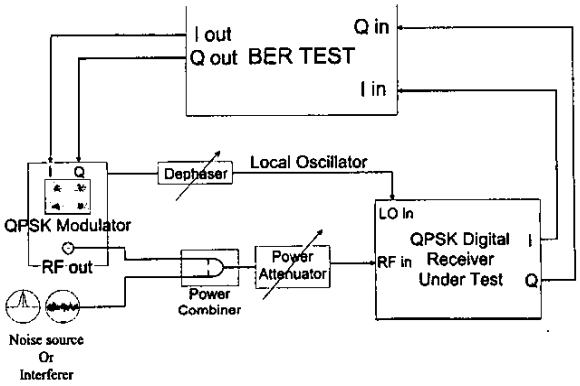

Fig. 3. Block diagram of the test bench set-up.

All measurements were made at 40 Mbps, well below the upper limit of both demodulators so as to guarantee a well behaved but high speed operation.

III. Performances Results

A. Noise

A typical BER measurement as a function of E_b/N_0 was made on both receivers as shown in Fig. 4.

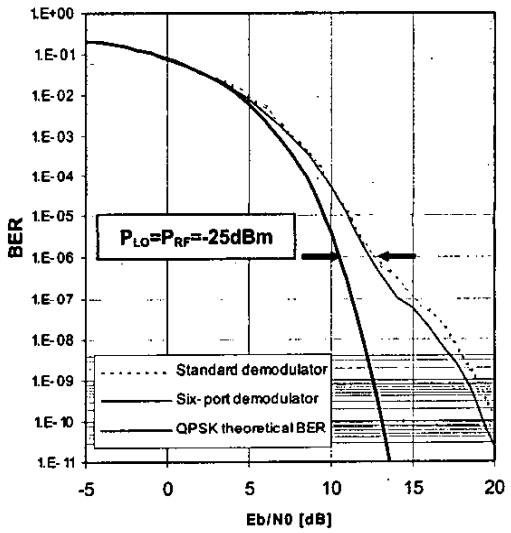

Fig. 4. Measured BER vs. E_b/N_0 for the two receivers operating at 40Mb/s with simulated QPSK BER waterfall curve.

At –25dBm LO and RF input power both receivers obtain good BER results with a slight advantage for the SPDR as seen in Fig. 4. For 10^{-6} BER both receivers are

only 2dB from the theoretical QPSK probability of error curve.

B. Receiver Sensitivity

BER measurements were made as a function of the RF power level at the input ports of both digital receivers with –25dBm LO power level and 40Mb/s data rate as seen on Fig. 5.

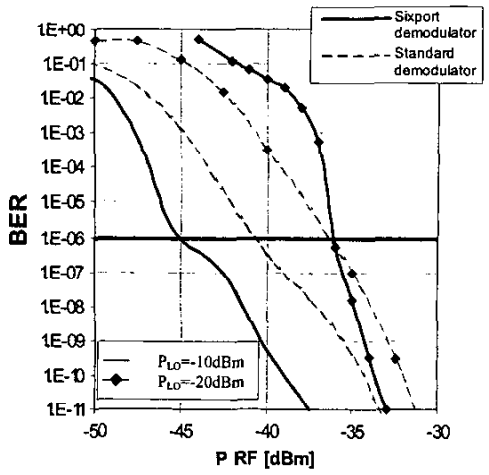

Fig. 5. Measured BER vs. RF input power level of both receivers for two LO input power levels (-10dBm & -20dBm) at 40Mb/s data rate and –65dBm noise level.

At –20dBm LO power, an advantage for the standard demodulator can be seen for BER values greater than 10^{-6}.

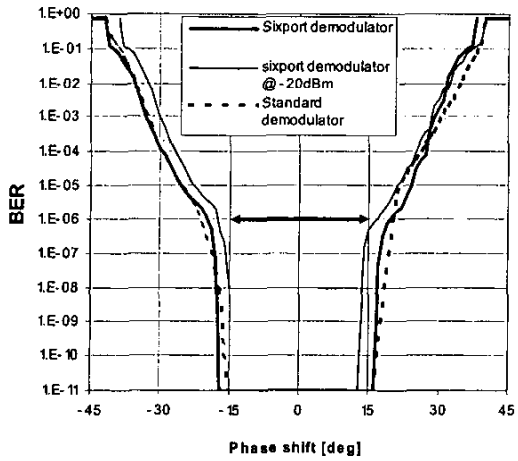

Fig. 6. Measured BER vs. local oscillator phase shift from synchronism (0°) at –10dBm LO power level (and –20dBm for the SPDR as specified) and 40Mb/s data rate.

At –10dBm LO power, the contrary happens: the SPDR becomes better in terms of sensitivity with respect to low RF input power levels: 4dB advantage at 10^{-6} BER.

LO phase shift is an important parameter to consider for the robustness of the carrier recovery and phase noise tolerance of LO. Phase shift results presented in Fig. 6 show a similar performance for both demodulators over more than 30° of total phase shift at 10^{-6} BER and –10dBm LO power level. Even at –20dBm LO power level the six-port's performance degrades only by a few degrees.

C. Interference Signals

Fig. 7 presents measurement results of BER versus the frequency difference between the carrier and CW interference at various power levels normalized to the power of the carrier.

It is hard to distinguish here the best performance: at 0dBc and +3dBc the SPDR has a slight advantage over the standard demodulator but at –6dBc the better sensitivity of the standard demodulator gives it a better performance, only at BER values above 10^{-3}.

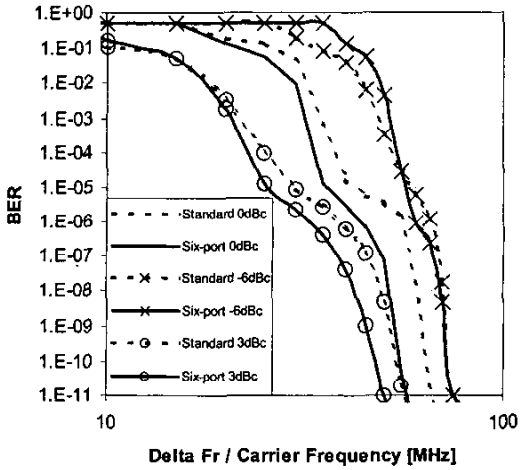

Fig. 7.Measured BER vs. frequency difference between carrier (2.45GHz) and a CW interference at 40Mb/s data rate for various interference signal power levels above carrier (dBc). Both demodulators are working in their typical conditions: PRF=PLO=-25dBm for the six-port receiver and PRF=-25dBm and PLO=-10dBm for the standard demodulator.

Fig. 8 shows the performance of both receivers for various power levels of an interference signal normalized to the main signal power level, and the interference is caused by a QPSK modulated signal at the same carrier frequency and the same data rate of 40Mb/s. The SPDR has a better performance than its standard counterpart with

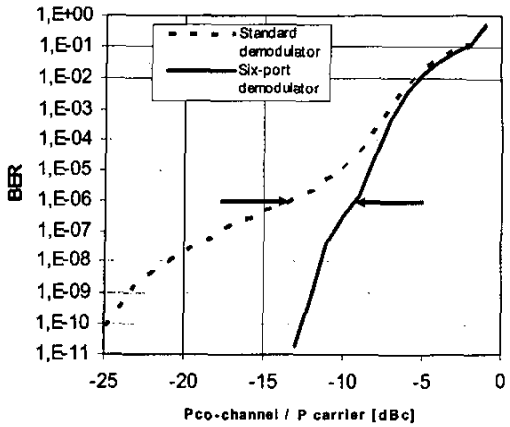

Fig. 8. Measured BER with co-channel interference, tests done under Fig. 7 conditions.

an advantage of at least 5dB of additional interference power level at 10^{-6} BER.

Fig. 9 gives BER measurements in the presence of a QPSK modulated interference signal at 40Mb/s whose frequency is set at 40MHz above the carrier frequency. Even with a strong channel interference (+6dBc) the six-port receiver is more robust and achieves a better performance. For equal power levels (0dBc) the SPDR has a 4 dB advantage over the standard receiver.

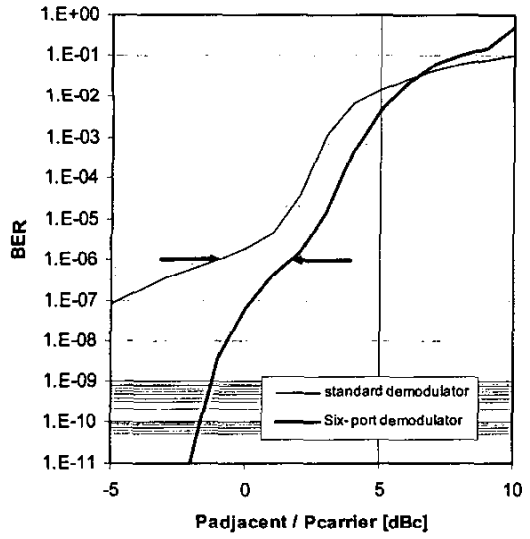

Fig. 9. Measured BER with an adjacent channel at data rate of 40Mb/s with carrier offset frequency of +40MHz, tests done under Fig. 7 conditions.

IV. CONCLUSION

Performances of six-port digital receiver and standard direct conversion receiver are presented. At least, similar or better performances in the presence of interference signals are achieved by the six-port circuits to provide a robust, low cost receiver with low power requirements. A MMIC implementation for an integrated front-end receiver can be facilitated by the architecture of six-port circuits.

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